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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,044	08/25/2000	CHANDRA V. MOULI	MIO 0054 PA	6800

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EXAMINER

NADAV, ORI

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 04/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/648,044

Applicant(s)

MOULI ET AL.

Examiner

ori nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 February 2002.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-14, 45 and 46 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14, 45 and 46 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 1/35/2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 02 February 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

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## **DETAILED ACTION**

### ***Drawings***

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 1/25/2002 and on 2/2/2002 have been approved by the examiner.

### ***Claim Objections***

2. Claims 1, 3, 12 and 45 are objected to because of the following informalities:  
The phrase "an ion implant concentration higher than remaining portions", as recited in claims 1, 3, 12 and 45 should read "an ion implant concentration higher than in remaining portions". The phrase "a pair of spaces adjacent the gate electrode, as recited in claim 6, should read should read "a pair of spacers adjacent the gate electrode".

### ***Claim Rejections - 35 USC § 102/103***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 3, 5-9, 11 and 45 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Pan (5,750,435)..

Pan teaches in figure 1e a circuit structure comprising a semiconductor layer 10; a source region and a drain region 24 in the semiconductor layer which are lightly doped and heavily doped with a first conductivity-type dopant; a channel region located between the source/drain regions; a gate oxide layer 14 located on a surface of the channel region; and a gate electrode 16 (column 5, lines 39-42) comprising polysilicon and one or more additional layers selected from the group consisting of metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks) having a defined leading edge located on the gate oxide layer, the portion of the gate oxide layer which is beneath the gate electrode and adjacent the leading edge and adjacent the drain region, and which defines an overlap region, having an ion implant concentration higher than in adjacent oxide layer portions comprising fluorine which can be effective to lower the surface electrical field in the overlap region (column 6, lines 37-44), and including a pair of spaces adjacent the gate electrode.

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Pan does not explicitly state that the fluorine is effective to lower the surface electrical field in the overlap region. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use fluorine in Pan's device sufficient to lower the surface electrical field in the overlap region in order to improve the device characteristics.

Regarding claim 11, Pan teaches in figure 1e a pair of conductive studs 28 and an interlevel dielectric layer 26 provided on the semiconductive layer, the interlevel dielectric layer have a pair of through bores, each accommodating one of each the pair of conductive studs, and one of each the pair of conductive studs contacting one of each the source/drain regions.

***Claim Rejections - 35 USC § 103***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 2, 4, 12-14 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan.

Pan teaches substantially the entire claimed structure, as applied to claim 1 above, except using a fluorine concentration of about  $1 \times 10^{18}$  atoms per cubic centimeter.

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Regarding claims 2, 4, 13 and 46, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a fluorine concentration of about  $1 \times 10^{18}$  atoms per cubic centimeter in Pan's device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claims 12-14, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Pan's transistor in a CMOS configuration in order to use the device in a specific application which requires a CMOS device.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pan (5,750,435) in view of Admitted Prior Art (APA).

Pan teaches substantially the entire claimed structure, as applied to claim 1 above, except a gate electrode is comprised of a layer of polysilicon, a layer of titanium nitride deposited on the polysilicon layer, and a layer of tungsten deposited on the titanium layer. APA teaches in figure 1 a gate electrode is comprised of a layer of polysilicon 18, a layer of titanium nitride 20 deposited on the polysilicon layer, and a layer of tungsten 22 deposited on the titanium layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a gate electrode comprising of a layer of polysilicon, a layer of titanium nitride deposited on the

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polysilicon layer, and a layer of tungsten deposited on the titanium layer in Pan's device, in order to reduce the contact resistance of the device.

8. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan (5,750,435) in view of Motoyoshi et al. (JP 6-53492).

Pan teaches substantially the entire claimed structure, as applied to claim 1 above, except using the transistor in a CMOS configuration.

Motoyoshi et al. use a transistor having a gate oxide comprising fluorine in a CMOS configuration. it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Pan's transistor in a CMOS configuration in order to use the device in a specific application which requires a CMOS device.

### ***Response to Arguments***

9. Applicant argues on page 8 that Pan does not teach an ion implant concentration in a leading edge and adjacent the drain region being higher than in adjacent oxide layer portions, because the ion implant concentration is substantially the same in the oxide layer except for the unhardened portion of the gate oxide directly underneath the gate electrode.

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Pan teaches a gate oxide comprising an ion implant concentration in a leading edge adjacent the drain region, and an unhardened portion of the gate oxide directly underneath the gate electrode which does not include substantial ion implant concentration. Therefore, Pan teach an ion implant concentration in a leading edge and adjacent the drain region being higher than in adjacent oxide layer portions, as claimed.

### ***Conclusion***

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of



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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772**.

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Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Ori Nadav

March 27, 2002

Steven Loke  
Primary Examiner

A handwritten signature in cursive script that reads "Steven Loke".